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BLIND DFE AND PHASE CORRECTION

FIELD OF THE INVENTION

The present invention relates to digital communication methods and systems.

BACKGROUND OF THE INVENTION

Modems for digital communications systems are designed to cope with various channel impairments. An essential element of the modem is the start-up process in which modem parameters such as equalizer taps, carrier frequency error, timing error, and gain setting, are estimated in order to provide the required modem performance.

In the prior art, two training modes are used: 1) using a known transmitted data sequence; 2) or using the transmitted information data without any prior knowledge of the value of the transmitted data. The latter mode is known as a blind start-up.

In the prior art, it is difficult to perform a blind start-up process, with limited computational resources and to converge to a good initial setting of the modem parameters for channels that exhibit severe linear distortion which gives rise to severe inter-symbol interference (ISI), and channels that suffer from severe narrow-band interference.

Therefore, there is a need in the art to provide a solution for the blind start-up process of a receiver in the context of digital communications signals in the presence of severe ISI and severe narrow-band interference. There is an additional need in the art to provide relief from ISI and severe narrow-band interference for conventional blind and non-blind modems.

SUMMARY OF THE INVENTION

The present invention is a method and apparatus for a digital communication receiver which is capable of operating over channels with severe ISI and narrow-band interference in either blind or non-blind modems.

The receiver of the present invention receives an analog signal modulated with digital information. The receiver converts the analog signal to a digital signal and demodulates the digital signal to recover the complex valued

components of the transmitted digital signal. The complex valued components are low pass filtered and passed through an adaptive pre-equalizer filter to reduce eigen value spread correlation.. The filtered complex valued signal is then subjected to a decision feedback equalizer which operates using a series of adaptive filters to additionally remove artifacts of inter-symbol interference. The resulting filtered and equalized complex valued signal is the converted to a digital signal to recover the digital information.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 depicts a digital communications system which employs the invention in a preferred embodiment.

Figure 2 describes the transmitter in the preferred embodiment of Figure 1.

Figure 3 describes the structure of the receiver in the preferred embodiment.

Figure 4 describes the operation of the pre-equalizer filter unit of the receiver in the preferred embodiment.

Figure 5 describes operation of the DFE (Decision Feedback Equalizer) in the receiver of the preferred embodiment.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural, logical and electrical changes may be made without departing from the scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present inventions is defined only by the appended claims.

Reference is made to Figure 1 which illustrates a typical application of a digital communications system operating over UTP (Unshielded

Twisted Pair) copper cables plant 102 or another communication medium such as coaxial cable. The present invention is applicable to many types of communication mediums, and in particular to a digital subscriber loop of a telephone network or a coaxial cable television infrastructure. The system comprises a transmitter 101 that receives a sequence 104 of data bits b[n], and outputs a signal x(t) to the cable. A wired communications medium 102, such as a copper cable plant, connects the transmitter 101 to the blind receiver 103. The blind receiver 103 receives a signal y(t) from the communications medium 102 and outputs a sequence of detected digital data bits $\hat{b}[n]$ 105.

The communications medium or cable plant may have one or more unterminated wire drops 106, as illustrated in Figure 1, and these wire drops may cause severe reflections that distort the signal and introduce significant inter-symbol interference (ISI).

FAS B17 Reference is made now to Figure 2, which describes the structure of the transmitter 101. In figure 2, the single-lined arrows indicate the propagation of real valued signals and the double-lined arrows indicate the propagation of complex valued signals. Real valued signals are a subset of complex valued signals and thus whenever the term "complex valued" is used herein, it encompassed either imaginary or real valued signals or the combination of the two which is a complex valued signals. The transmitter 101 operates according to a general approach of linear transmission that particularly include any one of PAM (Pulse Amplitude Modulation), QAM (Quadature Amplitude Modulation), PSK (Phase Shift Keying), CAP (Carrierless AM-PM), and NRZ (Non-Return to Zero) transmission methods, among others. The input data bits sequence b[n] is converted to a sequence of I-Q complex valued symbols, a[n], by a bit-to-symbol conversion unit 201, that may comprise a scrambler, a differential encoder, a trellis or a block FEC (Forward Error Correction) encoder, a CRC error protection encoder, a framer, a shell mapper, and/or protocol layer units.

The sequence a[n] is then fed to a cascade of transmission filter 202, an up-converter 203, where it is multiplied by sine and cosine sequences

that are generated in the sine wave source 204, a Digital to Analog (D/A) converter 205, an analog LPF (Low Pass Filter) 206 whose cutoff frequency is designed to reject aliasing effects of the D/A, and an amplifier 207. The output of the transmitter is the analog signal x(t).

Reference is now made to Figure 3 which illustrates the structure of the blind receiver 103. The input to the blind receiver is an analog signal y(t) that has propagated through the wired communications medium 102, such as a copper cable plant. This signal may suffer from severe reflections and linear distortions and it may contain a high level of noise and interference components due to e.g. narrow-band radio transmissions which occupy the same frequency band of the signal y(t).

The receiver input signal is low-pass filtered by the LPF 301 which is designed to combat sampling aliasing effects, then it is amplified by an amplifier 302 whose gain is automatically adjusted with an Automatic Gain Control (AGC) to exploit the dynamic range of sampler, and then the signal is sampled by Analog to Digital converter (A/D) 303. The sampling phase of the A/D is adaptively controlled by a timing PLL (phase locked loop) 304, which adjusts the sampling phase so that the power of the A/D output is maximized. Those skilled in the art will readily recognize that the timing PLL 304 may alternatively employ other conventional timing methods, such as decision directed timing.

The A/D output sequence is then down-converted by multiplying it with sine and cosine sequences that are synthesized in a sine wave source 305, and the resulting I and Q components are low pass filtered by the LPFs 306 and 307. Both LPFs 306 and 307 are designed to remove the demodulation image, to remove out-of-band signals, and to match the response frequency of the cascade of the transmission pulse response of transmit filter 202 of a typical cable plant or other communication medium 102 upon which the system operates.

The LPF units' outputs are then processed by a pre-equalizer filter unit 310, whose operation is described below in conjunction with Figure 4, and a Decision Feedback Equalizer (DFE) unit 308, whose operation is described

below in conjunction with Figure 5. The output of the DFE unit 308 is a sequence of detected I-Q symbols $\hat{a}[n]$ and an equalized sequence $s_5[n]$. These sequences are then processed by a symbol-to-bits conversion unit 309 that performs the inverse function of the bits-to-symbols conversion unit 201 and may employ a descrambler, differential decoder, FEC decoders, deframer, shell demapper, and/or a protocol layer decoder. The output of this unit is a sequence of the detected data bits $\hat{b}[n]$ 105.

Figure 4 illustrates the pre-equalizer filter unit 310. The input sequence of the unit, $s_1[n]$ is filtered by a digital FIR (Finite Impulse Response) filter 401 with L taps $p_n[1]...p_n[L]$ ($L \geq 0$) where $p_n[l]$ denotes the l-th tap after n iterations. The taps of the filter are adaptively adjusted by an adaptation unit 402. The adaptation rule is:

$$p_{n+1}[l] = p_n[l] + \Gamma_n\,(s_2[n])s_1^*\,[n-l] \qquad l = 1 \ldots L$$

where $s_2[n]$ is the output of the FIR filter 401, and where $\Gamma_n(x)$ is a possibly nonlinear function 403 whose parameters may vary with the iteration index n. A recommended class of Γ function is:

$$\Gamma_n\,(x) = \delta_p[n] \bullet x$$

where $\delta_p[n]$ $n = 1,2,...$ is a sequence of step sizes. The signal undergoes the following transformation:

$$s_2\,[n] = s_1[n] + \sum_{l=1}^{L} p_n[l]s_1[n-l] \quad (L \geq 0)$$

The input signal for the pre-equalization filter unit 310 is denoted $s_1[n]$ in Figure 4 and is routed to the FIR filter 401, the adaptation unit 402 and to summation circuit 404. $s_1[n]$ is combined with the output of the adaptive FIR filter 401 to produce the output signal $s_2[n]$ of the pre-equalization filter unit 310. The non-linear circuit 403 modifies the $s_2[n]$ signal to provide the feedback to adjusting the taps if adaptive FIR filter 401.

JAS A1 Figure 5 illustrates the DFE (Decision Feedback Equalizer). The DFE's input sequence $s_2[n]$ is first rotated by an adaptive rotator 501, by an

angle $\theta[n]$. The rotated sequence is then filtered by an FFE (Feed Forward Equalizer) FIR filter 502 whose taps' values are $c_n[1]..c_n[M]$ ($M \geq 1$), to produce output signal $s_3[n]$. Signal $s_3[n]$ is then summed 507 with the output of an adaptive FIR filter 504 whose taps are $d_n[1]..d_n[N]$, $N \geq 0$, and which is driven by the sequence of detected symbols $\hat{a}[n]$. The result of this summation is equalized sequence $s_5[n]$, 506. The sequence 506 is fed to a symbol detector 503 that employs a memoryless nearest neighbor decision rule, based on the transmitted symbols' I-Q constellation to generate the sequence $\hat{a}[n]$. We note that in this preferred embodiment, a single memoryless decision rule is employed. However, the present invention can be employed in a receiver that employs a more accurate detection scheme such as an approximate nearest sequence detector which is the maximum likelihood sequence estimator when the noise of the input of unit 503 has a Gaussian distribution.

The parameters of units 501, 502 and 504 are jointly updated by $S_5[n]$ to combat ISI (Inter-Symbol Interference) and noise. The adaptation scheme is the following:

$$\theta[n+1] = \theta[n] + \rho_n(s_5[n])$$
$$c_{n+1}[m] = c_n[m] + \varphi_n(s_5[n])s_3^*[n-m] \qquad m = 1...M$$
$$d_{n+1}[i] = d_n[i] + \Psi_n(s_5[n])\hat{a}^*[n-i] \quad i = 1...N$$

where $\rho_n(x)$, $\varphi_n(x)$, and $\Psi_n(x)$ are possibly nonlinear complex valued scalar function whose parameters may depend on the iteration index n, and $M \geq 1$, $N \geq 0$.

The adaptation functions in this embodiment are:

$$\varphi_n(x) = \begin{cases} \delta_c[n]\left(x - \hat{a}(x)\right) & n > T_2^c \\ \delta_c[n]\left(|x|^2 - k_1\right)x & T_1^c \le n < T_2^c \\ \delta_c[n]\left(\mathrm{Re}^2(x) - k_2\right)\mathrm{Re}(x) & n < T_1^c \end{cases}$$

$$\rho_n(x) = \begin{cases} \delta_\theta[n]\left(\mathrm{Re}^2(x) - k_2\right)\mathrm{Re}(x)\,\mathrm{Im}(x) & n < T_1^\theta \\ \delta_\theta[n]\,\mathrm{Im}\left(\hat{a}(x)x^*\right) & n \ge T_1^\theta \end{cases}$$

$$\Psi_n(x) = \begin{cases} \delta_d[n]\left(x - \hat{a}(x)\right) & n > T_2^d \\ \delta_d[n]\left(|x|^2 - k_1\right)x & T_1^d \le n < T_2^d \\ \delta_d[n]\left(\mathrm{Re}^2(x) - k_2\right)\mathrm{Re}(x) & n < T_1^d \end{cases}$$

where $\delta_c[n]$, $\delta_d[n]$ and $\delta_\theta[n]$, $n = 1, 2, \ldots$, are sequences of real-valued step sizes, where k_1 and k_2 are real valued scalars, and where Re(-) and Im(-) denote the real part and the imaginary part of a complex scalar, and where $\hat{a}(x)$ is the result of a memoryless nearest neighbor symbol detector whose input is x. T_1^c, T_2^c, T_1^θ, T_1^d and T_2^d are positive scalars.

The sequences $s_1[n] \ldots s_5[n]$, $\hat{a}[n]$ may be calculated at the symbols rate (T-spaced receiver). Alternatively $s_2[n]$, $s_3[n]$ and $s_4[n]$ may be calculated at a higher rate (Fractionally spaced receiver). The resulting outputs of units 501, 502 and 504 are described as follows:

$$s_3[n] = s_2[n] \bullet e^{j\theta[n]}$$

$$s_4[n] = \sum_{m=1}^{M} c_n[m] s_3[n-m]$$

$$s_5[n] = s_4[n] + \sum_{l=1}^{N} d_n[l]\, \hat{a}[n-l]$$

CONCLUSION

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This patent is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.